Nano-RF is a European project and the main concept is the development of CNT & graphene based advanced component technologies for the implementation of miniaturized electronic systems for 2020 and beyond wireless communications and radars.

The developed components and technologies developed during the project will be implemented in the following *demonstrators*:

- Reflect array antennae for wake vortex and weather radars

- Graphene receiver module

The demonstrators will exhibit the reconfigurability, systemability, integratability and manufacturability of the developed technologies and unify advanced More-than-Moore elements and Beyond-CMOS devices with existing technologies. It addresses "System Perspective" to support miniaturized electronic systems for 2020 and beyond.

This Nano-RF newsletter intends to present the latest progress obtained during last year of the project.

Design and Simulation activities

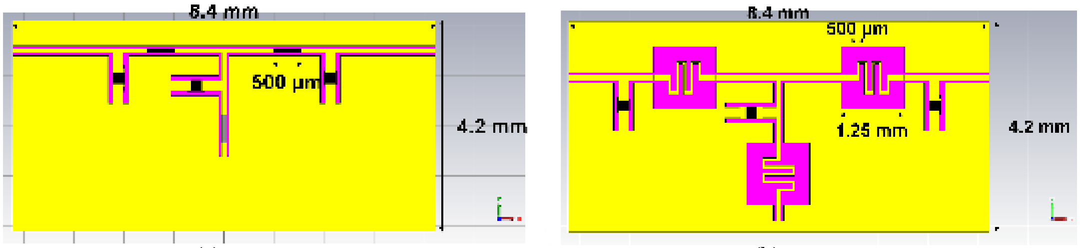
➢ Design of CNT filter

We report the design and results of the simulations carried out with CST Microwave Studio® (CST MWS) for the optimization of the CNT-based tunable microwave (MW) band-pass filter.

The layout is very compact and exploits:

1. three wires (diameter of 25 µm, length of 1 mm) in parallel for the inductors on the coplanar waveguide (CPW) signal (100 µm-wide), or three meander inductors;
2. Three CNT-based varactors (same as first fabricated filter).

Fig. 1a shows the new filter with wire-based inductors, whereas Fig. 1b displays the filter with meander inductors.



(a) (b)

Figure 1 : CST MWS design (with main dimensions) of the new compact CNT-based tunable MW band-pass filter with: (a) wire inductors; (b) meander inductors.

The two configurations are 4.2-mm wide and 8.4-mm long. This substantial miniaturization provides small MW metal (gold) losses; furthermore, the CNT growth process is also improved with respect to the first prototype.
CPW dimensions are already in agreement with standard measurement probe tips. Namely, the gap/signal/gap (G/S/G) dimensions are 50/100/50 µm, respectively.
The technical details of the filters are:

- molybdenum in the IDTs area for CNT growth has a thickness of 50 nm;
- gold for CPW signal and ground deposition has a thickness of 1 µm, to prevent from skin depth effects;
- the inductance of each wire is about 5.121 nH, so that the inductance of 3 wires in parallel is about 1.707 nH (it could be possible to use up to 5 wires to tune the inductance value); the inductance of each meander is about 0.92 nH.
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As in the case of the first prototype, the biasing technique can be realized via the CPW by simply applying a "+" to the signal and a "-" to the ground, respectively.
Fig. 2a shows the electromagnetic simulations of the filter with wire inductors (modeled as thin perfect electric conductor – PEC – components) in terms of return loss |S11| and transmission |S21|, whereas Fig. 2b provides the simulation results for the filter with meander inductors. In both cases, we considered only the presence of the IDTs without CNTs. Each IDT exhibits an estimated capacitance value of 0.387 pF, so that the presence of the CNTs is expected to modify the overall varactor capacitance (hence, tuning the filtering frequency) according to the applied DC bias voltage.

Table I summarize and compares the performance of the two solutions.

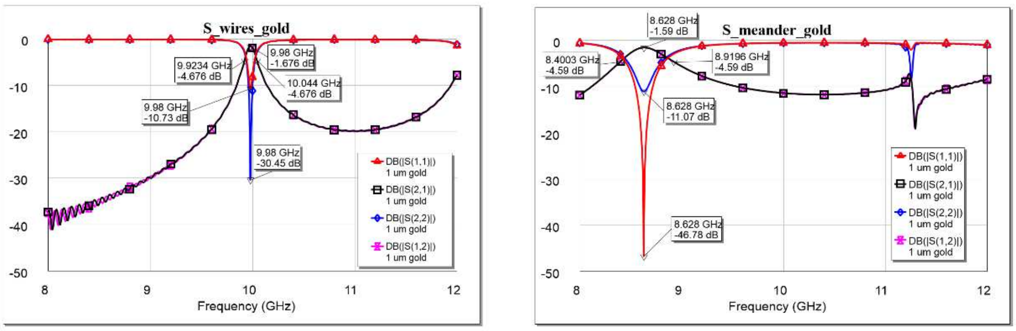
Table 1: main performance of the two proposed CNT-based tunable MW band-pass filters.

Performance	Layout with wires	Layout with meanders
Filtering frequency	9.98 GHz	8.63 GHz
|S11|/|S22|	-10.73/-30.45 dB	-46.78/-11.07 dB
Insertion loss	1.68 dB	1.59 dB
Bandwidth (-3 dB)	120 MHz	519 MHz
Q-factor	617	489

From Table I, it is apparent how the layout with wires offers the best performance in terms of bandwidth and Q-factor.

Finally, Fig. 3 shows the simulations (for the filter with meander inductors) performed with AWR to verify how |S11| and |S21| change by putting in parallel to the each IDT scattering matrix a lumped element (capacitor) emulating the CNTs effect. The significant thing is that AWR provides a fast method to test if changing the overall varactor capacitance affects the performance of the filter. In detail, by assuming a capacitance of 0.2 pF for each CNT matrix, we observed a downshift of the filtering frequency of about 500 MHz.

The fabrication steps are the same as reported last year and will be not reproduced here again. The masks production and devices fabrication will be performed at Thales France, whereas for the wire inductors we expect to solder the wires at IMT Bucharest, in order to verify the overall effect of the wires themselves on the filtering performance.



(a) (b)

Figure 2: EM simulation results (performed by means of CST MWS) for the new compact CNT-based tunable MW band-pass filter with: (a) wire inductors; (b) meander inductors.

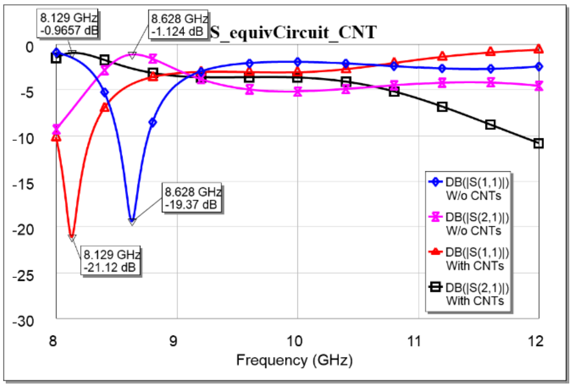


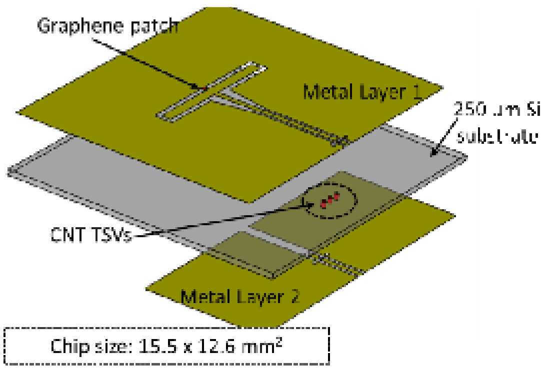
Figure 3 : AWR simulated return loss and transmission, without and with CNTs, for the new compact CNT-based tunable MW band-pass filter with meander inductors and CNTs capacitance of 0.2 pF. The downshift of the filtering frequency is evident.

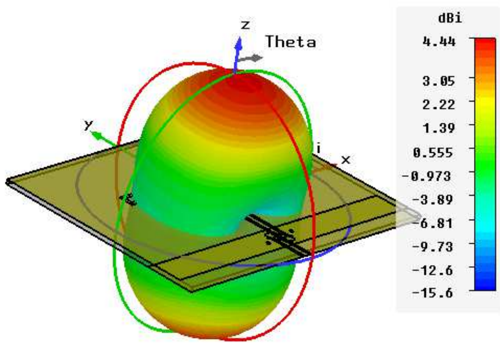
➢ Design of Graphene antenna coupled with CNTs TSV interconnect

This work is performed to demonstrate the integration of graphene antenna with TSV CNT to demonstrate the integration of the antenna into a MMIC which is a thorny issue in many cases.

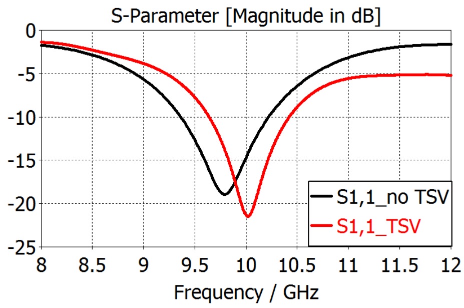
The X band slot antenna loaded with a 200x200 µm2 square graphene patch described in D4.4. was further adapted for flip-chip integration using CNT TSVs. The CNT TSVs have a diameter of 200 µm and can be processed in a 250 µm thick silicon substrate. The initial design of the antenna considered on-wafer probing and bond wire integration and had the gap-signal-gap widths of the input coplanar waveguide (CPW) of 50-100-50 microns, with a ~50 Ω line impedance for a 525 µm thick high-resistivity (ρ~5000 Ω·cm) silicon wafer. To accommodate the CNT TSVs the input CPW was widened to 150-300-150 microns. The thinning of the substrate also meant a redesign of the antenna altogether, with the final size of the chip of 15.5 x 12.6 mm2. Three CNT TSVs are placed on the input CPW transmission line and connect the front side CPW with the backside. The 3D expanded model of the antenna with graphene patch and CNT TSVs is shown in Fig.x.1.(a). The 3D radiation characteristic is shown in Fig.x.1.(b), with a simulated directivity of 4.4 dBi at 10 GHz and two main lobes. A comparison between the reflection losses of the initial antenna design (black trace) and the antenna with CNT TSVs (red trace) is shown in Fig.x.1.(c).

➢





(a) (b)

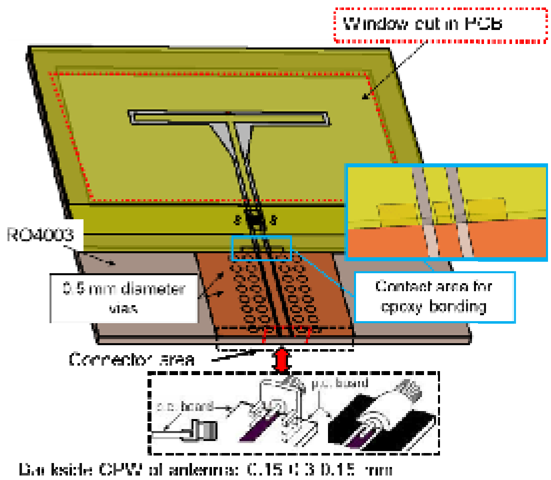


(c)

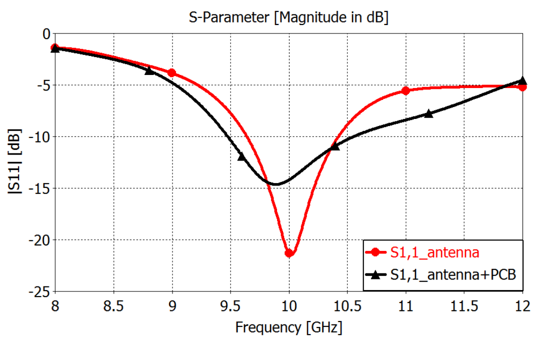
- **Figure 4: X-band graphene antenna integrated with CNT TSVs: (a) schematic; (b) 3D radiation characteristic at 10 GHz (directivity); (c) comparison of |S11| parameter for the initial antenna with graphene patch (black trace) and for the antenna with additional TSV and backside transition (red trace)**

- The antenna can then be bonded directly using silver epoxy on a PCB. The PCB substrate chosen for integration was RO4003 (Rogers), which is a low loss material suitable for X band operation (εr=3.55; tanδ=0.0027 @10 GHz; substrate thickness 0.406 mm; copper cladding 17 µm). A window will be cut under the antenna so as not to interfere with the radiation characteristic. The coplanar waveguide on the PCB is computed for 50 Ohm characteristic impedance and is grounded using two rows of vias on each side of the signal line. These vias ensure limited leakage. At the end of the PCB a standard SMA connector can be mounted, as described in Figure 5.(a).

- A 3D electromagnetic model of the antenna with CNT TSVs, integrated on the RO4003 PCB was developed and simulated. A comparison between the reflection losses of the antenna with CNT TSVs and the integrated antenna is shown in Figure 5(b). There is a slight influence which should not impede the proper operation of the antenna.



(a)



(b)

- **Figure 5: Integration of antenna with graphene patch and CNT TSV on a PCB: (a) schematic; (b) comparison of |S11| parameter of the antenna and the antenna integrated with the PCB**

Fabrication and Test activities

➢ CNTs devices fabrication and characterization

- CNT switch

A test set was built to measure the switching behavior of the Carbon-Nano-Tube (CNT).

The CNT do not stands large currents; a large resistor is needed to limit the DC current. We made the test with a 50MegOhm. Figure 6 present a schematic of the experimental set-up

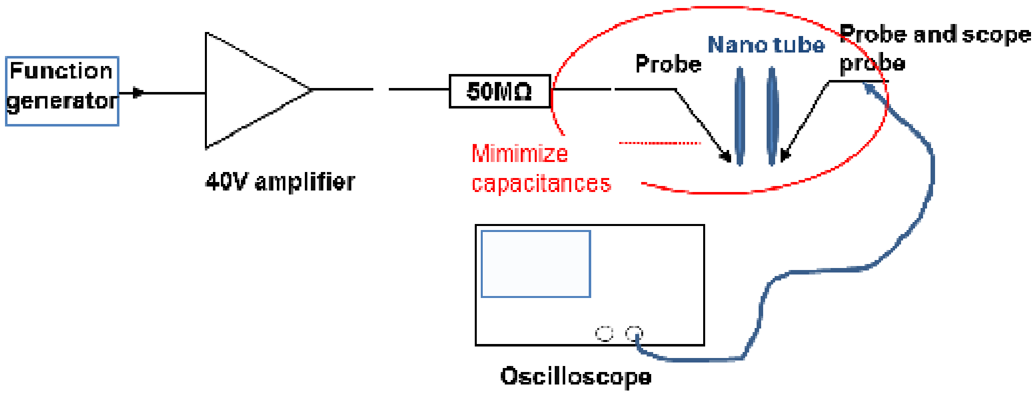


Figure 6 : test set description

A function generator provides the chosen wave shape and it is amplified up to tens of volts.

An oscilloscope is used to measure the waveforms. The scope has a very large memory, so we can store the whole waveforms and analyzed them later. The waveforms can also be read by the spice simulator, so we can fit the circuits values and behavior.

It is required to limit the parasitic capacitance in the test implementation and especially the capacitances after the 50MegΩ and on the measurement side.

The DC current will be limited by the 50MegΩ and the scope10MegΩ. When switching, the current is not limited except by the CNT resistance.

The available energy is set by the parasitic capacitance between the 50MΩ and the probe to ground (i.e the baseplate on which the sample is placed).

On switching, this energy will flow very quickly to the measurement probe and scope probe capacitances.

Figure 7 shows a picture of the set up used for the DC measurement with probes, 50Mohm resistance and the scope probe

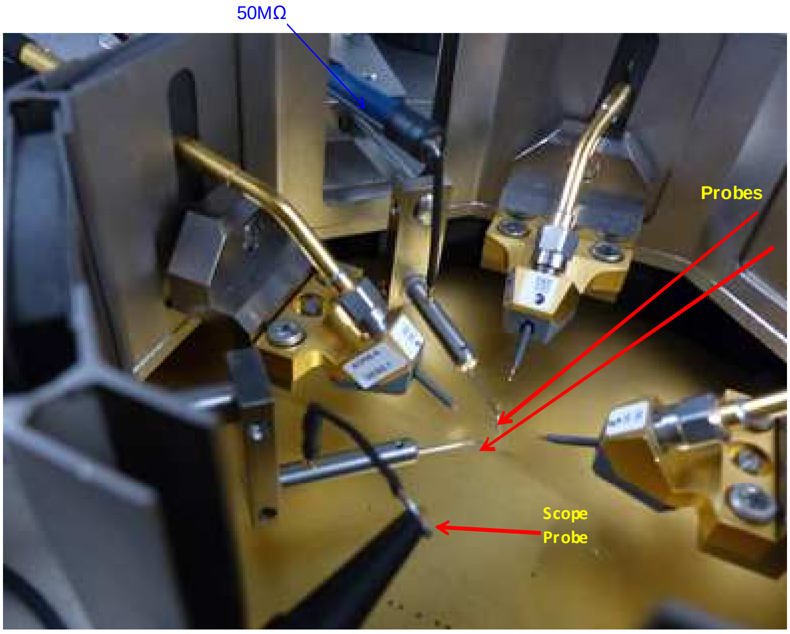


Figure 7 : picture of the probes and resistor Nota the RF probes are not used

The critical point for the measurement on the CNT DC switch is the parasitic capacitance which can cause the destruction of CNTs. The parasitic capacitance before the CNT switch is identified with preliminary measurements. The scope probe is typically 10pf and 10MegΩ. Rough order of magnitude of the current may be:

if we have 25V and a CNT resistance of 25kΩ, this is 1mA peak and it decreases to 0.5mA in ~0.12µs. (this may lead to the CNT destruction). Figure 8 show a schematic of the different capacitance

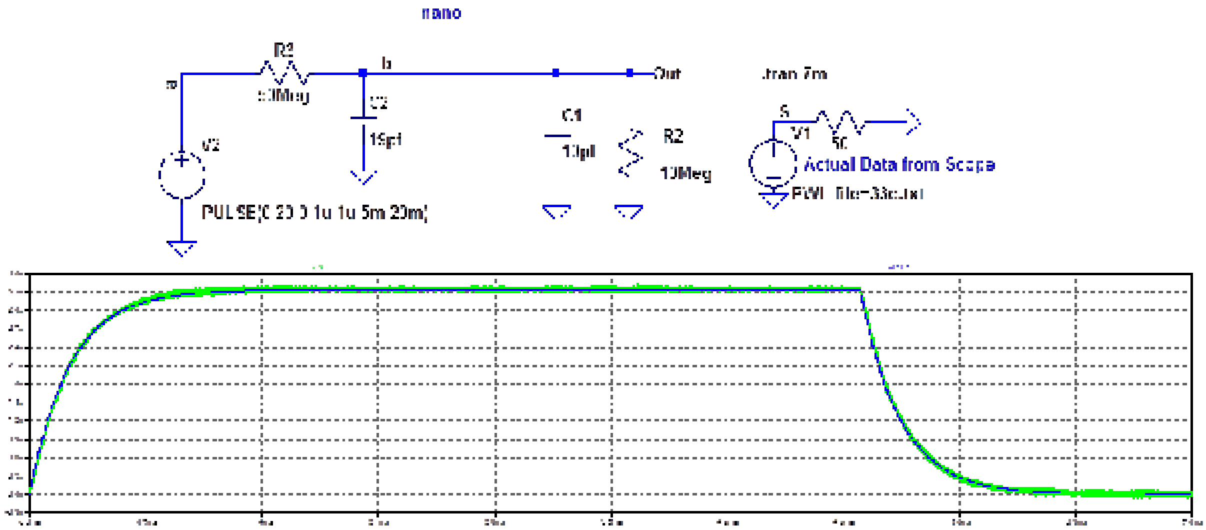


Figure 8 : Identification of the capacitance

Several measurements have been done using this experimental set-up and two successive actuations have been observed. Results are summarized on Figure 9

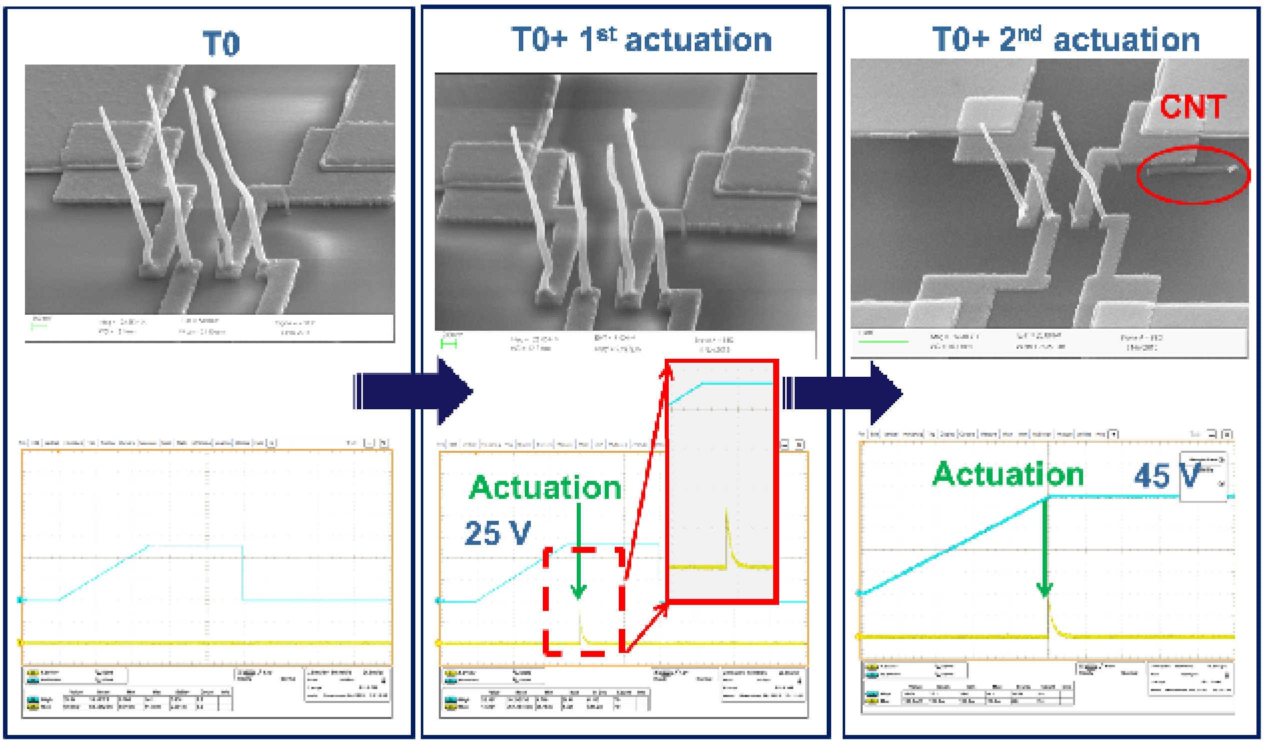


Figure 9 : Observation of two actuations on the same DC switch device

At 25 V, we observe a peak corresponding to a first actuation between 2 CNTs of middle. SEM observations show a reduction of the CNTs height and validate the actuation. Same measure on the same device is performed and a second activation is observed at 45V. The difference can be explained by the fact that CNTs are shorter and therefore requires a higher voltage for activation. As before, destruction CNT is observed (one is shorter and one moved out of the electrode)

This has been reproduced on several devices and the same behavior is observed.

- <u>CNT interconnect</u>

The proposed process is illustrated as figure 1 has shown. The CVD-grown MWCNT bundles (Figure 10 (a)) were partially densified on the upper half part. Therefore a funnel-shape CNT bundle (Figure 10 (b)) was formed. In parallel, the via was etched (Figure 10 (c)) on the chips by deep reactive ion etching (DRIE), and a layer of thermal release tape was attached on the front surface of the via chip as the transfer medium (Figure 10 (d)). The upper part densified CNT bundles were aligned to the via and launched down to the tape by flip chip bonder (Figure 10 (e)). The CNT bundles with root part undensified were kept in the via (Figure 10 (f)) due to the adhesive strength between the CNT bundles and the tape when the donor silicon is lift up and removed. The second round densification was performed (fig. 1(g)), where after polymer was filled into the gap between chip and CNT bundles (Figure 10 (h)). The overburden of polymer was flattened (Figure 10(i)) by chemical mechanical polishing (CMP). Hereafter the thermal release tape was released (Figure 10 (g)).

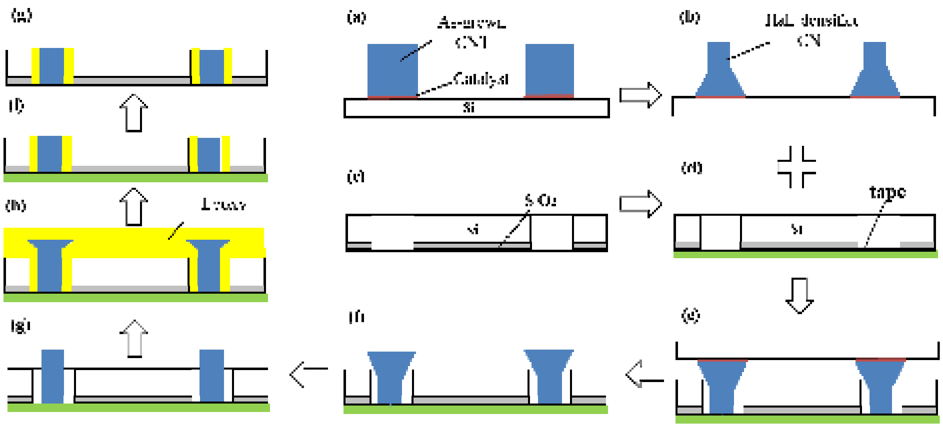


Figure 10 : Schematic of process flowchart

The principle of densification on CNT bundles by solvent is that capillary forces stemming from the exposure to solution will squeeze together the sparsely located CNTs, thereby increasing the density of CNTs in the bundle by reducing its cross-sectional area. To improve the controllability of the CNT bundles shape, a vapor phase densification method was introduced in some papers, where solvent vapor is condensed onto the surface of the CNT bundles, instead of immersing CNT bundles into the solvent. The pristine CNT bundles are placed upside down over a bath of 1:1 mixture of acetone and water, heated to 100 °C. Since the densification rate depends on the condensation rate on the CNT bundles, i.e. on the vapor pressure of acetone, the vapor pressure has to be controlled. This was done by confirming variables affecting the vapor pressure and fixing them, so that all parameters except time is kept constant. The following parameters were confirmed to affect the rate of densification, and corresponding are the method to keep them stable and uniform.

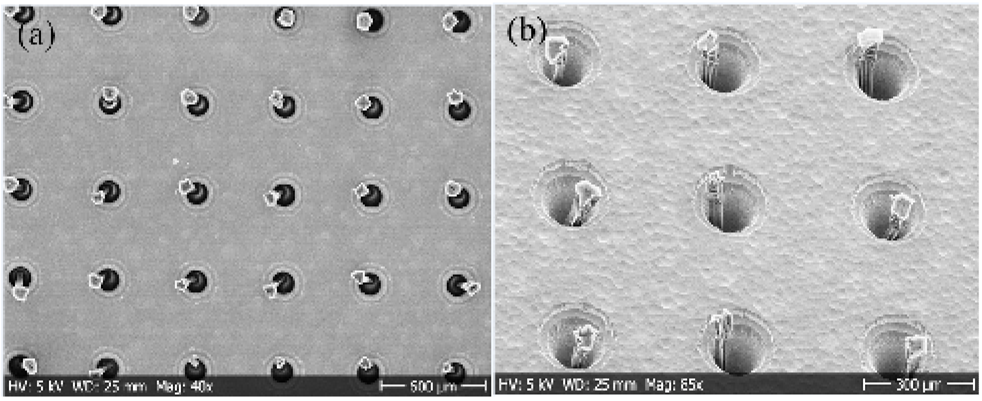


Figure 11 : (a) MWCNT bundles were transferred into the via and second densification was performed to shrink the root part of the bundle. (b) The close-up of the SEM photos of figure 5(a).

By comparing the different degrees of densification, it can be clearly seen CNT bundles of 20 s exposure to the vapor solvent is best configuration for the scenario of double-densification transfer. Because on the one hand, the diameter of upper top part of CNT bundles was shrunken to 20 ~ 30 µm, which make it possible to insert the CNT bundles to the smaller via; On the other hand, along with the upper half densified part, the undensified lower half part of the CNT bundles make the whole CNT bundles funnel shape structure, which is quite robust to withstand external force interference. In this point, 20 s densification is selected for the following transfer into the via. When inserting of upper half densified CNT bundles into the via, as long as the upper top part of the CNT bundles slide into the via, the undensified root part of the CNT bundles would be squeezed inward mechanically by contacting the wall of the via. With the same setup of the first round densification, the porous root part of the CNT bundles were densified as shown in Figure 11(a) and Figure 11(b). After the second densification, the gap between the CNT bundles and the wall of the via needs to be filled with curable epoxy. The purpose of polymer filling is to help fix the CNT bundles after curing and form a robust structure for the following CMP planarization process of back surface of substrate. This epoxy layer can also work as the insulation layer, which could reduce capacitive coupling and increase the reliability of TSV compared to conventional silicon oxide.

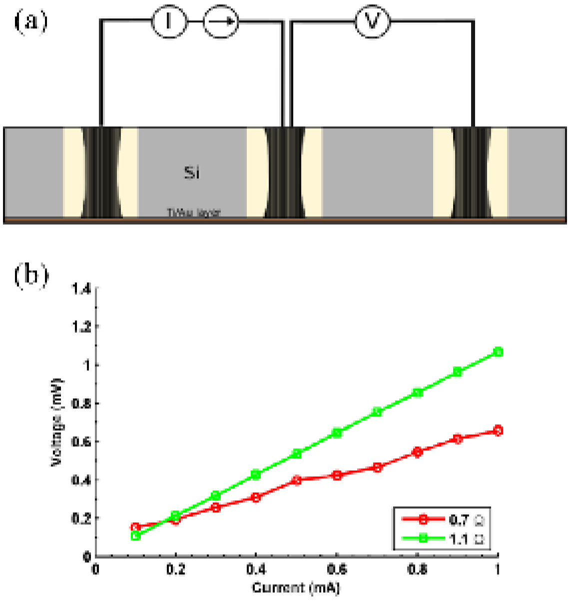


Figure 12 : (a) Illustration of the four-probe measurement. (b) DC I-V response for CNT TSV.

In order to measure the electrical conductivity of the CNT interconnects, 20 nm Ti and 300 nm Au were sputtered onto the back surface of the sample. The configuration of measurement by four probes method was illustrated as Figure 12(a), and three CNT TSVs were utilized for extracting one resistance of CNT TSV. The electrical resistance was found to be between 0.7 Ω and 1.3 Ω. If the whole CNT bundle was assumed to be a cylinder with average diameter around 30 µm and thickness of the 280 µm, the resistivity of the CNT bundles is calculated to be 2 ~ 3 mΩ cm

➢ Graphene devices fabrication and characterization

• Graphene Growth

There are several ways to obtain graphene material and we started to study the different graphene synthesis methods.

- **SiC decomposition**

Based on LiU work aims in the Nano RF project, we have developed our growth conditions to increase the size of graphene/SiC from 7×7mm2 to 15×15 mm2 and 20x20 mm2 by having full control on the epitaxial graphene growth process on SiC and obtain cm scale continuous coverage of ML (monolayer) graphene. To reach the aims during the reported period a series of graphene samples were grown on the Si face of 4H SI SiC in an inductively heated furnace at a temperature ranging from 1700-1950°C, in argon ambient with a pressure range from 750 - 950 mbar, in Si rich ambient, and at different growth times. As the buffer layer is a precursor for graphene formation and can strongly influence its quality; depending on the buffer layer the integrity of the graphene may contain defects. Graphene formation was analyzed in respect to step bunching and surface decomposition energy differences created by the SiC basal plane stacking sequence on SiC polytypes. We showed that buffer layer halts step bunching process (Fig 1a) on 4H and 6H-SiC, which means surface energy becomes uniform all over the substrate surface after coverage by a buffer layer and subsequently resulting in uniform and continuous ML coverage. In Fig. 1a 100% means full coverage with buffer layer and the excess value is ML coverage.

The results from graphene samples grown at different argon ambient pressure show that there is an optimal argon pressure yielding a large coverage of ML graphene (Fig 1b). We demonstrate that the same optimal argon pressure holds for graphene growth at different temperatures and both Si and C-rich conditions at which a max monolayer graphene coverage takes place (Fig. 1b).

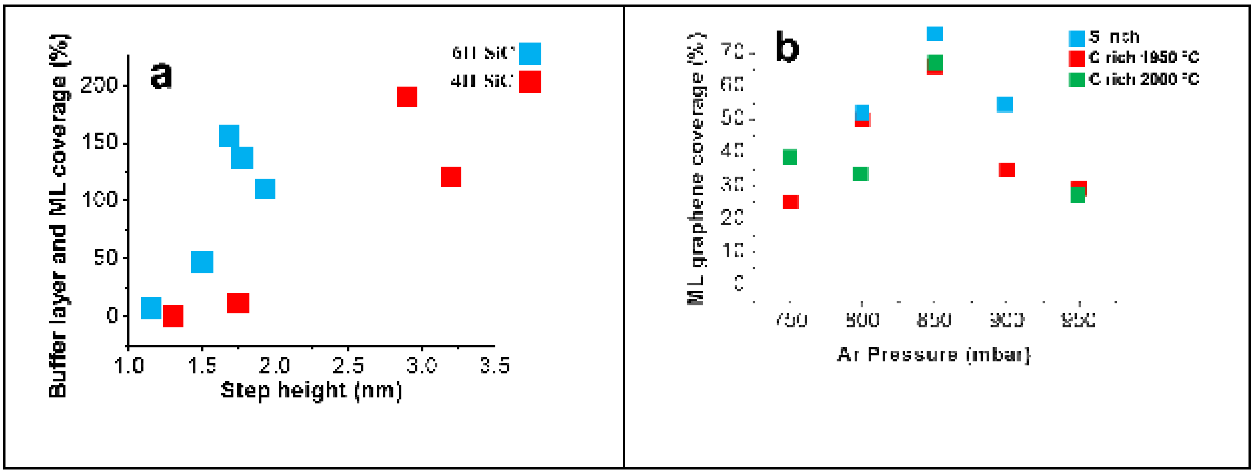


Figure 13 : a) Step height vs. buffer layer and ML coverage, b) ML graphene coverage vs. Ar pressure.

The temperature dependence of the buffer layer and ML graphene coverage is sublinear, which means the formation process is surface kinetics limited (Fig. 2a). The time dependence of ML and bilayer graphene growth shows (Fig. 2b) that graphene spreads faster on 4H-SiC substrates from the start of the growth, and ML coverage increases approximately linearly with increasing growth time. After ML completion the growth time does not have a pronounced effect on enlargement of the bilayer graphene area for both 4H and 6H-SiC polytypes.

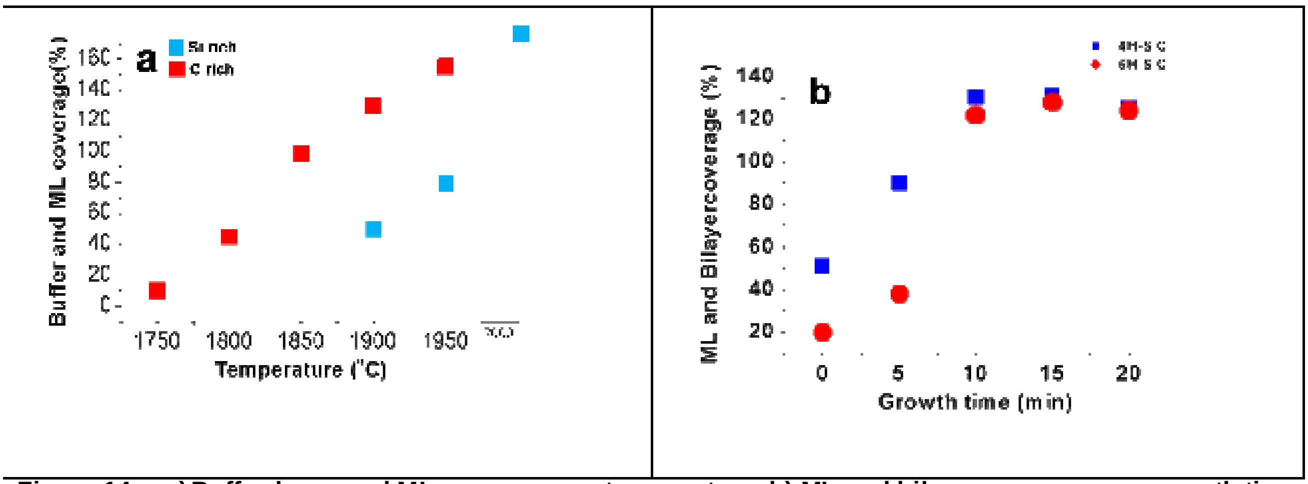


Figure 14 : a) Buffer layer and ML coverage vs. temperature, b) ML and bilayer coverage vs. growth time

Based on the above results we were able to develop our growth conditions to increase the size of SiC samples from 7×7 mm2 to 20×20 mm2 (Figure 15). We have elaborated a growth protocol for graphene on 15x15mm2 and 20×20 mm2 SiC substrates on which ~99% ML area can be obtained Figure 15, we have also increased ML graphene reproducibility up to 98 % for 7×7mm2 samples.

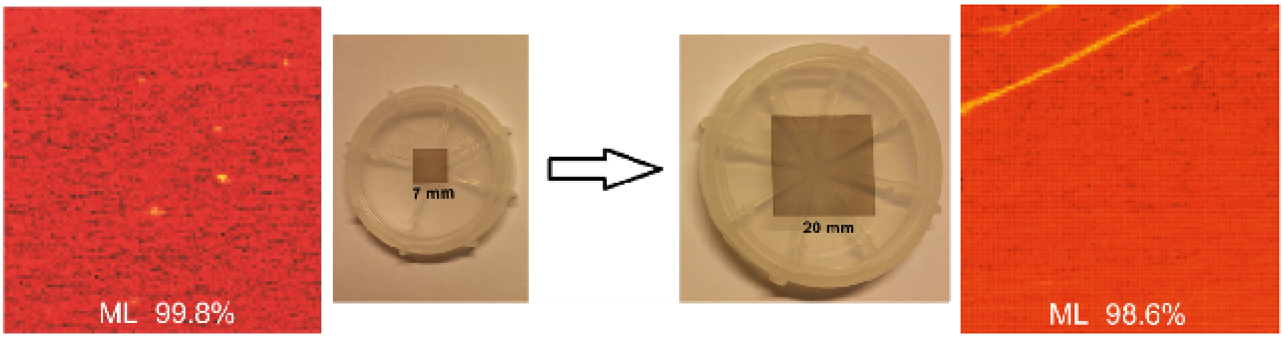
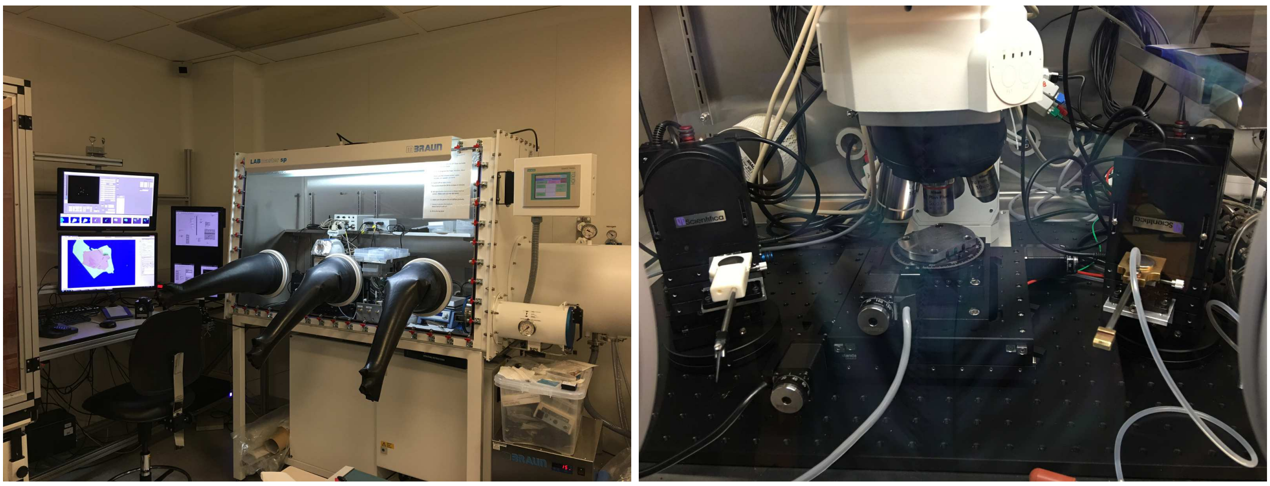


Figure 15: Increasing the size of SiC samples from 7×7 mm^2 to 20×20 mm^2 with large area continues ML coverage.

Furthermore, we have shown that formation of nitride interface is a method to modify the electronic properties of graphene on SiC, which can be applied for intercalation and chemical doping. Our modeling results, using first principles calculations, demonstrate that nitrogen intercalation is a promising way to access charge neutral graphene on a semiconducting surface.

- <u>Graphite ex-foliation (GI)</u>

During this period (T+36M → T+45M) there were no requests from consortium partners for monocrystalline graphene flakes. So instead of preparing additional graphene samples, we allocated time to enhancing our system for manipulating graphene and other 2D crystals within an inert atmosphere. The system consists of a fully motorised microscope and a pair of manipulators within an argon glovebox, as shown in the two photographs below:



The atmosphere is under continual purification to maintain water and oxygen concentrations below 0.1 ppm. Both water and oxygen can contaminate or otherwise degrade a wide range of 2D crystals, particularly those that are chemically unstable in air such as black phorphorus (2D semiconductor) and niobium diselenide ($NbSe_2$, 2D superconductor). Our system can be used to transfer 2D crystals on top of each other to create van der Waals heterostructures [1] – materials with novel properties.

Nano-RF Publications

In the last 12 months the partners of the Nano-RF project published various results related to the project.

- Publications
  - M. Dragoman, A. Dinescu, D. Dragoman, Room temperature on-wafer ballistic graphene field-effect-transistor with oblique double-gate Journal of Applied Physics 119, 244305 (2016); doi: 10.1063/1.4954639
  - M.Dragoman, Carbon-based nanodevices routes: inks, flakes, spaghetti, wafers-invitated papers 8th International Conference on Advanced Materials, ROCAM 2015.
  - M.Dragoman, Receiving microwave signals with graphene-invited paper , WOCSDICE ,Smolenice, 2015.
  - D. Mencarelli, S. Bellucci, A. Sindona, L. Pierantoni, Spatial dispersion effects upon local excitation of extrinsic plasmons in a graphene micro-disk Article in Journal of Physics D, Applied Physics, October 2015.
  - D. Mencarelli, L. Pierantoni, M. Stocchi, and S. Bellucci, Efficient and versatile graphene-based multilayers for EM field absorption Applied Physics Letters 109, 093103, 2016.
  - Sun, S., et al, Vertically aligned CNT-Cu nano-composite material for stacked through-silicon-via interconnects, Nanotechnology, 27 (33), 335705, 2016.
  - Sindona, A., Pisarra, M., Mencarelli, D., Pierantoni, L., Bellucci, S., Plasmon modes in extrinsic graphene, Ab initio simulations vs semi-classical models, NATO Science for Peace and Security Series B: Physics and Biophysics, pp. 125-144, 2016.
  - Xin Jin[1], James. C. M. Hwang[1], Davide Mencarelli[2], Luca Pierantoni, Marco Farina[2] Calculating tip-sample capacitance and charge density of a near-field scanning microwave microscope, *accepted* to IEEE Magazine
  - N.M. Caffrey, R. Armiento, R. Yakimova and I.A. Abrikosov, PHYSICAL REVIEW, B 92, 081409(R) (2015)

- Conference
  - A.Dinescu, M.Dragoman, A.Avram, Scanning electron microscopy for nanoscale characterization and patterning of graphene devices, 16th Nanoscience and Nanotechnology Conf. , Frascatti, 2015-invited paper.
  - M. Dragoman, M. Aldrigo and A. Radoi, Switching microwaves with 2D materials, MEMSWAVE Barccelona, Spain, 2015.
  - M. Aldrigo, A. Stefanescu, M. Dragoman and D. Vasilache, Enhancement of capacitive RF MEMS switches reliability based on a carbon nanotubes array embedded in the dielectric, MEMSWAVE Barccelona, Spain, 2015.

- M.Dragoman, The sinuous path of electromagnetic waves in 2D materials inks, flakes,islands and flatlands, invited paper , 11 International Conference on Optics, Micro-nanophotonics IV ROMOPTO 2015, Romanian Academy, p. Bucharest, 2015.
- M.Dragoman, 2D materials nanotechnologies between great expectations and lost illusions, invited paper, 3rd International Conference on Nanotechnologies and Biomedical Engineering,, p.47 , Chisinau, Moldova (2015).
- A.C. Obreja, S.Iordanescu, R.Gavrila, A.Dinescu, F. Comanescu, A.Matei, M.danila, M.dragoman, H. Iovu, Flexible films based on graphene/polymer nanocomposite with improved electromagnetic interference shielding, 38 th IEEE CAS Conference, Sinaia, Romania,p.49-52, 2015.
- M. Aldrigo, M.Dragoman, L.Pierantoni, D.Mencarelli, and G. Deligeorgis, Back-gate bias of a graphene antenna via a smart background metallization, 38th CAS Conference , Sinaia, Romania, p. 131-134, 2015.
- Mencarelli, D., Pierantoni, L., Rigorous simulation of ballistic graphene-based transistor, IEEE MTT-S International Microwave Symposium Digest, 2016-August, 7540140.

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